A Flexible Computer Architecture and Tools for CENG Computing Projects

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Motivation

The Computing Challenge

- Fundamental physical limitations
- Increasingly specialized hardware needed for continued performance scaling.

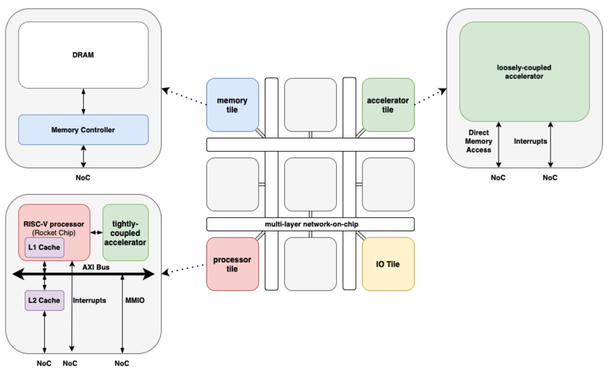
Open-Source Hardware

- Hardware is entering an open-source renaissance (ISAs, CAD tools, processors, and libraries).
- Lack of support for advanced hardware techniques
- Ad hoc hardware development to date

Need for a flexible, unifying hardware development framework for emerging computing applications.

RAMP Framework

The RAMP framework allows for rapid development of custom-tailored Systems-On-Chip, leveraging modern open-source tools.



An open-source System-on-Chip design framework, surrounding modular processor, memory, IO and accelerators.

Hardware Goals

Advanced Techniques

- Energy Efficiency
- Full System

Extendibility

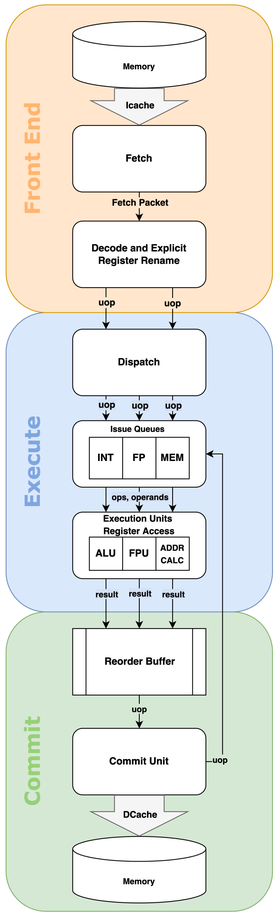
- Modular Design
- Integrated Testing
- Formal Methods

Targets

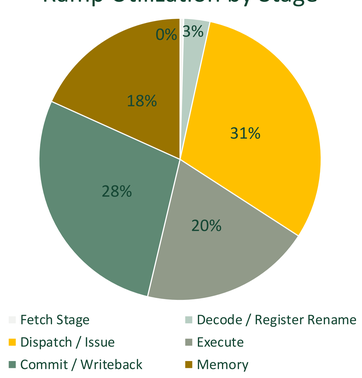
- FPGA with DRAM
- AWS Cloud Instance
- VLSI tools

RAMP CORE

*RAMP Core's **out-of-order**, **superscalar** design allows for multiple instructions to be executed simultaneously, greatly increasing performance.*

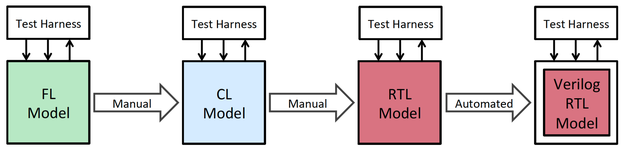


Ramp Utilization by Stage



RAMP RISC-V Superscalar Processor

- An open-source, out-of-order (OoO) RV32I processor, for use in the RAMP framework.
- Leverages advanced hardware techniques.
- **First OoO RISC-V processor to use PyMTL3**



	RAMP CORE	OTTER Pipelined	OTTER Multicycle
Pipelined	Yes	Yes	No
Multi-Issue	Yes	No	No
Dynamic Scheduling	Yes	No	No
Branch Prediction	Yes	No	No

Open-Source Hardware Tools

PyMTL3

- An open-source Python framework for hardware **modelling**, **generation**, **simulation** and **verification**.
- Multi-level development paradigm lowers barrier to entry for non-specialists, and allows for more rapid development and experimentation

Python Packages

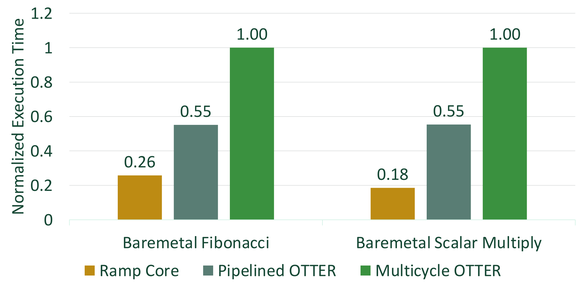
- Python base will introduce tools previously detached from hardware research.
- **jupyter, pytest, hypothesis, numpy**

Verilator

- Powerful, lightweight open-source Verilog simulation and testing solution.
- Tightly integrated with PyMTL3 for unit testing.

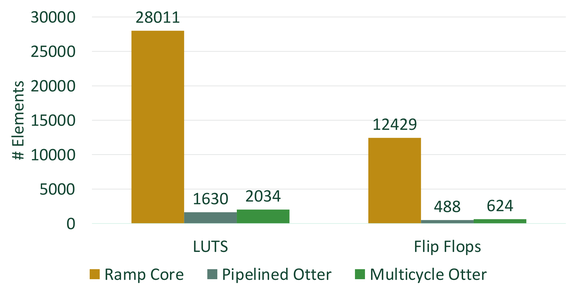
Results

Performance

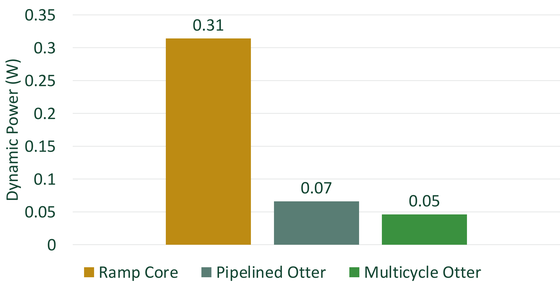


*RAMP Core provides a **3x** speedup over Pipelined OTTER and over a **5x** speedup over Multicycle OTTER running bare metal benchmarks.*

Area



Power Consumption



***6x** increase in power over Pipelined OTTER. Within embedded/IoT power-budget (<1W). Optimizing area and power subject for future work*

Summary

- RAMP Core outperforms all of Cal Poly's current processors in bare-metal benchmarks, provides researchers access to more advanced hardware techniques.
- RAMP Core's extendible, configurable design and centralized repository provide a robust framework for future education and research into modern computing solutions.