Curtis Bucher

949.922.4198 | cpbucher5@gmail.com | www.curtisbucher.com
https://www.linkedin.com/in/curtisbucher/ | www.github.com/curtisbucher

EDUCATION

California Polytechnic State University **June 2024**
Bachelor of Science, Computer Engineering
Magna Cum Laude **President's Honor List** **3.8** GPA

RELEVENT SKILLS

Languages: SystemVerilog, UVM, Python, C, RISC-V Assembly
Applications: Linux, OOP, Cadence Indago, Git / Github, Perforce
Technical Interests: Computer Architecture, Design Verification, DV Tooling, Programming Language Design

EXPERIENCE

OpenAI **Jan 2026 - Present**
Member of Technical Staff - Design Verification

Apple **August 2024 – Jan 2026**
Design Verification Engineer – Pixel Processing

- Implement and maintain UVM IP-level and subsystem level testbenches for verifying Apple's SOCs using constrained random verification
- Work closely with designers to root cause complex RTL failures
- Manage detailed testplans for systematically defining and verifying desired chip behavior with coverage mapping
- Developed and maintain a package to automate UVM scoreboard integrity checks with negative checking

Apple **April 2023 - Sept 2023**
Design Verification Intern – CPU

- Implemented a unified design verification framework to verify multiple Apple CPUs, requiring less time and compute than previous independent implementations.

Cal Poly University **June 2022 – Mar 2023**
Student Researcher

- Started a research group of undergraduates, graduates, and faculty to design and implement a flexible SOC design framework, leveraging open-source tools.
- Taped out a RISC-V SOC using an open-source toolchain, including Verilator, Icarus Verilog, CocoTB, OpenLane, Yosys, and Slang.

Blue Marble Communications **June 2021 – Dec 2021**
Software Engineering Intern

- Tested optical satellite modems and transceivers on an interdisciplinary team of engineers.
- Wrote unit tests in C to automatically analyze production code for embedded FPGA hardware.

PROJECTS

Senior Project *https://curtisbucher.com/assets/files/pydve.pdf*

- Designed and implemented a novel Python-based design verification framework for hardware emulation.

RAMP Core *https://cal-poly-ramp.github.io*

- Worked independently with engineering faculty in the SURP program to design and implement an open-source, superscalar, out-of-order RISC-V processor targeted at research and education.

Capstone Project *https://poly1rover.com/index.html*

- Designed a space-rated small-scale Mars Rover with an interdisciplinary team of undergrads.
- Led team to implement hardware accelerator for robot arm kinematics

ACTIVITIES

CPython *Volunteer Contributor*

- Implemented union operator for Python chainmaps in PEP 584.

For up-to-date information, please visit my website, www.curtisbucher.com or GitHub account. References available upon request.